REMARKS/ARGUMENTS

Claims 1-32 are pending in the present application.

This Amendment is in response to the Office Action mailed February 11, 2004. In the Office Action, the Examiner rejected claims 1-26 under 35 U.S.C. §112; and claims 1-32 under 35 U.S.C. §103(a). Applicant has amended claims 1 and 14. Reconsideration in light of the amendments and remarks made herein is respectfully requested.

Rejection Under 35 U.S.C. § 112

1. In the Office Action, the Examiner rejected claims 1-26 under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Applicant has amended claims 1 and 14 to clarify the claim language as suggested by the Examiner.

Therefore, Applicant respectfully requests the rejection under 35 U.S.C. §112 be withdrawn.

Rejection Under 35 U.S.C. § 103

1. In the Office Action, the Examiner rejected claims 1-2, 14-15, and 27-28 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,237,064 issued to Kumar et al. ("Kumar") in view of U.S. Patent No. 6,047,348 issued to Lentz et al. ("Lentz"); claims 3-13, 16-26, 29-32 under 35 U.S.C. §103(a) as being unpatentable over Kumar in view of U.S. Patent No. 6,629,218 issued to Cho ("Cho"), further in view of Lentz, and further in view of U.S. Patent No. 6,438,657 issued to Gilda ("Gilda"). Applicant respectfully traverses the rejection and contends that the Examiner has not met the burden of establishing a prima facie case of obviousness.

Applicant reiterates the arguments set forth in the previously filed Response to the Office Action.

Kumar, Cho, and Gilda were discussed in the previous response.

Lentz discloses a system and method for supporting a multiple width memory subsystem. A subsystem writes to a main memory by either a 32 or 64 bit data transfer. It transfers data in a "double pumped" fashion (Lentz, col. 4, lines 61-64). Lentz merely discloses double pumping data bus, not control signals. Lentz even states that double pumping may cause bus conflict

when the buses turn around and switch from one master to a new master (Lentz, col. 5, lines 1-4). This indicates that Lentz does not suggest to use double pumping for control signals.

Kumar, Cho, Lentz, and Gilda, taken alone or in any combination, does not disclose, suggest, or render obvious controlling a cache memory in a memory controller via double-pumped or quad-pumped control signals. There is no motivation to combine Kumar, Cho, Lentz, and Gilda because none of them addresses the problem of controlling a cache memory using a controller internal to a processor. There is no teaching or suggestion that the control signals being double pumped or quad-pumped is present. Kumar, read as a whole, does not suggest the desirability of putting the chipset cache in a memory controller.

Furthermore, if the proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. In re Gordon, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984). MPEP 2143.01.

Here, Kumar does not disclose or suggest the cache being internal to a memory controller. Moving the cache into the memory controller would render Kumar's circuit unsatisfactory for its intended purpose. The intended purpose of Kumar's technique is to reduce cache latency by paralleling various memory accesses by the execution unit (Kumar, col. 3, lines 42-44). Kumar specifically provides two separate buses: a backside bus (BSB) and a frontside bus (FSB) associated with a BSB queue and a FSB queue, respectively (Kumar, col. 5-8). Kumar further teaches that the BSB queue tracks the memory requests submitted to the offchip L2 data array of the L2 cache, while the FSB queue tracks the memory requests submitted to the main memory (Kumar, col. 4, lines 9-13). Therefore, Kumar does not suggest to incorporate the L2 cache inside the memory controller because that would defeat the purpose of parallel operations. Cho merely discloses integrating the processors, the L2 cache, the memory controller, the I/O interfaces and bridges, etc. may be integrated onto a single circuit. However, Cho does not disclose or suggest a processor cache unit and a chipset cache controller internal to the processor and the control signals being double or quad-pumped.

Therefore, Applicant believes that independent claims 1, 14, 27 and their respective dependent claims are distinguishable over the cited prior art references. Accordingly, Applicant respectfully requests the rejections under 35 U.S.C. §112 and 35 U.S.C. §103(a) be withdrawn.

Conclusion

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

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